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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,773	KURAMORI ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Sep 26, 2003 asnd Mar 22, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03222004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "n21" is not shown in Fig. 2 (e.g. see page 10, lines 6, 13, and 18); and "n31" is not shown in Fig. 3 (e.g. see page 17, lines 6, 11, and 12). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicants will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The title of the invention, a "substrate voltage generating circuit", appears to describe an invention that is not clearly shown or disclosed with respect to how it can apparently generate a voltage (e.g. VBB) having a third potential lower than the second potential, as described later. A new title is required that is clearly indicative of the invention to which the claims are directed, and which is accurately shown/disclosed within the figures/disclosure. Therefore, it is suggested the title relate to what the examiner believes is the main critical feature of the application: a level shift circuit, with two transistors having thicker gate oxides than two other transistors within the level shift circuit.

The abstract of the disclosure is objected to because, like the title, the abstract appears to be describing a substrate voltage generating circuit that does not appear to be clearly shown or disclosed, with respect to being able to generate voltage VBB. It is suggested the abstract concentrate on the level shift circuit of the invention. Correction is required. See MPEP § 608.01(b).

The disclosure is objected to because of the following informalities: Page 3, line 20 to page 4, line 2, and page 16, lines 16-17, identify Fig. 3 as a "substrate voltage generating circuit", which is misleading. Although the figure shows a circuit that can be used within a substrate voltage generating circuit, the figure's circuit itself is a level shift circuit (e.g. see the description starting on page 16, line 19; page 18, lines 9-10; the description starting on page 18, line 17; and claim 9 which corresponds to the circuit shown in Fig. 3). Page 6, line 2 ".1.5 V" should be -- -1.5 V-- to clearly identify a negative voltage lower than voltage VSS. Page 8, lines 8 and 15 "sown" should be --shown-- to correct a typo. Page 8 (line 13) and 9 (line 2) should have --NAND-- instead of "NADN", thus correcting other typos. It is not understood how substrate voltage VBB is transferred to output node OUT.vbb when switch element SW1 is on as described on page 13, lines 14-17. For example, when SW1 of Fig. 1 is turned on, it would be obvious to one of ordinary skill in the art that VSS is coupled to OUT-vbb. Therefore, where does "VBB" come from? Related to the above problem, since nodes n1 and n2 are coupled directly to VSS, how can those nodes have substrate voltage VBB outputted from output node OUT.vbb as described on page 15, lines 15-18? The descriptions on pages 17-18, with respect to node "n31", are inconsistent. For example, page 17, lines 3-7 imply that node "n31" is the node between P31 and N31. However, page 17, lines 8-12, and page 18, lines 2-3, indicate the node is

between P32 and N32. Since "n31" is not even shown in Fig. 3, corrections and/or clarifications must be made to ensure the proper node(s) is (are) identified within the figure and disclosure. Also on page 17, are the sources of the two PMOS transistors P31 and P32 connected to distinct power supply nodes (as implied by "first power supply node" on line 5, and "second power supply node" on lines 9-10), even though they are both coupled to the same power supply voltage VDD? Page 19,line 17 should have one of the redundant terms deleted from "the the." Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-6 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a level shift circuit, does not reasonably provide enablement for a substrate voltage generating circuit. Therefore, the use of "substrate voltage generating circuit" within the preamble of claim 1 does not accurately identify the circuit being described within the claim. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. Although the applicants' own Fig. 1 is identified as a "substrate voltage generating circuit" that apparently generates substrate voltage VBB at its output terminal, the figure and disclosure do not clearly show/disclose how this is actually accomplished. For example, the right side terminal of both capacitors c1 and c2, as well as one terminal from each of NMOS transistors SW1 and SW2, are coupled directly to VSS. Therefore, when the gate of the

transistors receives a low signal VBB (through inverters INV1 and INV 2, respectively), the transistors will be off and VSS is not coupled to output terminal OUT_vbb. Also at this time, the left side terminal of capacitors c1 and c2 receive VDD (through inverters INV3 and INV 4, respectively), and would charge up towards VDD via the pull-up section of their respective inverter (e.g. INV 3 or INV 4). However when the outputs of inverters INV 1 and INV 2 transition from VBB to VDD, the gate of the corresponding transistor receives VDD, and the transistors turn on, coupling VSS to output terminal OUT_vbb. At this time, the left side terminal of capacitors c1 and c2 receive VSS (through the pull-down section of their respective inverter INV3 or INV 4), thus discharging the capacitor's previous charge towards VBB. Therefore, it is not understood how the claimed invention (e.g. related to the applicants' own Fig. 1) can be a substrate voltage generating circuit that apparently generates a third potential level (e.g. VBB), that is supposedly lower than the second potential level (e.g. VSS), at the output node (e.g. OUT_vbb). If the circuit within Fig. 1 doesn't actually generate VBB itself, but merely helps control its level (e.g. if VBB become more negative than desired, it needs to be raised up towards VSS to bring it back into an acceptable range), what actually generates VBB, and then apparently applies it to node OUT_vbb? Dependent claims 2-6 carry over the rejection from claim 1.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. It is not clear in claim 1 how the "output node receiving a voltage

having a third potential level" (lines 5-6), relates to the output node being connected to the second power supply node (lines 10-11), which is supplied with the "second potential level." For example, if the output node is connected to the second power supply node, wouldn't the output node have the second potential level instead of the third potential level (that is lower than the second potential level)? Also, since claim 1 is a substrate voltage generating circuit, how does the voltage at the output node relate to the implied substrate voltage the circuit apparently generates? The use of "having the first and second potential levels" and "having the first potential level and the third potential level" on lines 9 and 10-11, respectively of claim 1 are confusing. For example, do the signals alternate between these levels (e.g. as logic high and low type signals); have these levels as maximum/minimum levels of each signal (e.g. the signals can be between, or equal to, the levels); or just have these levels within a desired range of their respective signal? Claim 2, lines 6-7 are misleading with respect to the gate of the second transistor receiving the input signal. For example, as shown in the applicants' own Fig. 2, and its associated disclosure, the first/second transistors P1/P2 receive complementary input signals, not the same "input signal" as recited within claim 2. Claim 3 has the same type of problem as claim 2, wherein the first/second transistors do not receive the same "input signal" as the limitations on lines 3-4 and 6-7 imply. Since the basic structure of claim 3's level shift circuit corresponds to the circuit shown within the applicants' own Fig. 3, it is not understood if the gate oxide film thicknesses are accurate as currently recited. For example, lines 4-8 of page 18 indicate the thicknesses of the gate oxide film of the fifth/sixth transistors N33/N34 are actually thicker than those of third/fourth transistors N31/N32, wherein claim 3 recites they are thinner. Therefore, is the "thinner' limitation on lines 20-21 of claim 3 correct, or are the disclosed oxide thicknesses

on page 18 correct? Therefore, it is suggested that claim 3, or the disclosure, be corrected to provide consistency between the claimed limitations and the disclosed descriptions. Both independent claims 7 and 9 have the same "input signal" related problem as claims 2 and 3 described above (i.e. the first/second transistors do not both receive the same "input signal" as lines 2-3 and 5-6 of each of claims 7 and 9 recite). Also, claim 9 has the same gate oxide film related problem as described within claim 3 (i.e. the fifth/sixth transistors have a thinner gate oxide film than the third/fourth transistors as recited within the claim, or a thicker gate oxide film as disclosed on page 18).

Claims 8 and 10 each recite the limitation "The substrate voltage generating circuit" in line 1 with insufficient antecedent basis for this limitation in either claim.

No claim is allowable as presently written.

Allowable Subject Matter

However, claims 7 and 9 would be allowable if rewritten or amended to satisfactorily overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure the gate oxide thicknesses of the third/fourth transistors is thinner (or thicker?) than from the gate oxide thicknesses of the fifth/sixth transistors as recited within each of claims 7 and 9.

Also, claims 8 and 10 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. These claims depend on claims 7 and 9, respectively, which would be allowable as described above.

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed inventions. Fig. 7 of Taura et al. shows a six transistor level shift circuit that directly corresponds to the applicants' basic circuit structure shown in Fig. 2. Also, Taura et al.'s Fig 10, and Fig. 27 of Tokai, each shows another level shift circuit, with six transistors, that directly corresponds to the applicants' own Fig. 3 basic circuit structure. However, neither of these references clearly shows/discloses the gate oxide thickness of the third/fourth transistors as being different from those of the fifth/sixth transistors (as recited within claims 2-3, 7, and 9). Chang et al. shows a level shift circuit in Fig. 3, wherein transistors PG1-PG2 and NG1-NG2 are each understood to have a thick oxide, and transistors N1-N4 are each understood to have a thin oxide (e.g. see column 2, lines 40-43). This reference also discloses that thin oxide transistors are used within a core logic, and thick oxide transistors are used in input/output units (e.g. see column 1, lines 20-26 and column 4, lines 61-64); and the thin oxide transistors allow NMOS transistors to turn on sufficiently, because of their low threshold voltages, even when the input voltage is low (e.g. see column 2, lines 61-63). Column 4, lines 53-61 teach the substitution of thick oxide NMOS transistors "in the conventional voltage level shifter" with thin oxide NMOS transistors. However, there is no strong motivation to substitute only two of the four NMOS transistors within Taura's Figs. 7 and 10; Tokai's Fig. 27; or Tanaka's Fig. 5 (a) (described later) with thin oxide transistors, wherein two of the four transistors will have a gate oxide that is thicker (or thinner) than the gate oxides of the other two transistors. However, these references should still be reviewed and considered with respect to the basic six transistor configured level shift circuits.

The reference of Uchikoba et al. (Uchikoba) shows a substrate voltage generating circuit 10 in Fig. 1 comprising a first power supply node supplied with first potential level VDD; a second power supply node supplied with second potential level VSS < VDD; an output node receiving voltage VBB having a third potential level VBB lower than second potential level VSS (e.g. see Fig. 2); and level shift circuit 50,30,20 coupled between first power supply node VDD and the output node. Signals NBBUP and BBDOWN can be considered one type of input signal, that alternates between the first and second potential levels (e.g. see Fig. 2), that is received by at least one section (i.e. 30) of the level shift circuit. In Fig. 3, the reference shows switch circuit 41 that could be used instead of 40 shown in Fig. 1 (e.g. see column 11, lines 47-48). The Fig. 3 configuration connects second power supply node (i.e. VSS) to output node (i.e. VBB) in response to output signal NBBUP. However, this reference does not show an output signal from the level shift circuit that alternates between the first and third potential levels.

The prior art references cited on the IDS submitted Mar 22, 2004 were reviewed and considered. The reference of Tanaka et al. is of most interest. That reference's Fig. 5(a) level shift circuit corresponds to the applicants' own Fig. 2. Column 2, lines 65-67 indicate that MOS transistors not receiving 3.3 V between the gate and drain, or between the gate and source, have thin gate oxide layers; column 5, lines 19-33 cite the use of thick and thin oxide transistors; and column 5, lines 39-47 cite the setting of gate oxide thicknesses and threshold voltages with respect to circuits coupled to the input/output. However, column 6, lines 8-11 clearly disclose all the PMOS and NMOS transistors in Fig. 5(a) have a thick gate oxide, even though lines 2-5 indicate a total voltage difference of only 3.3 V. Therefore, this reference does not provide strong motivation for modifying Fig. 5(a) of this reference, or any of the other references cited

above, that shows/discloses level shift circuits (with a specific six transistor configuration), corresponding to the applicants' Fig. 2 or 3. The US Patent reference of Ryu shows/discloses a substrate voltage generating circuit, but lacks the level shift circuit for providing an output signal with first and third potential levels, and the switch circuit connecting the second power supply node to the output node, as recited within claim 1. The Japanese patent is by Ryu, and corresponds to Ryu's US Patent reference.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund
10 May 2005

TUAN T. LAM
PRIMARY EXAMINER